

REMARKS / ARGUMENTS

The applicant respectfully submits that the aforementioned amendments have been made to the patent application to correct typographical and other errors due to inadvertence. Furthermore, the applicant respectfully submits that the amendments do not add new subject matter to the application.

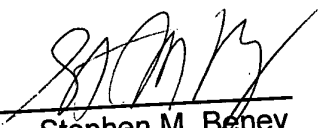
Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"Version with markings to show changes made."**

The applicant respectfully requests that these corrections be allowed in this case.

Respectfully submitted,

Bereskin & Parr

By


Stephen M. Beney
(416) 957-1697
Reg. No. 41,563

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the specification:

The paragraph beginning at page 28, line 9 has been amended as follows:

-- Referring now to Figure 26, an embodiment of the ~~coupler 66~~ of synchronization element 66 comprising transistor QC and the coupler 68 comprising ~~comprises a transistor QC and a capacitor CC is shown.~~ The transistor QC is used to modify the impedance of the antenna 50 couple energy from the test result signal 34 ~~through capacitor CC to the antenna 50 which is transmitted back to the test unit 12.~~ The source of the transistor QC is connected to the gate of the transistor QC such that the transistor QC acts as a resistor when enabled. The test result signal 34, for a given test state, is coupled to the source of the transistor QC. The transistor QC is enabled by an antenna couple enable signal 170 which is derived from a combination of the state signals S0 or S8 of sequencer 60, such as the logical XNOR of state signals S0 and S8, ~~since these signals have a digital value of '1' when there is no testing being done (i.e. refer to Table 1).~~ When the antenna couple enable signal 170 has a digital logic value of '1', the transistor QC is enabled which allows the test result signal 34 to be applied to the antenna 50 and radiated towards the test unit 12. When the antenna couple enable signal 170 has a digital logic value of '0', the transistor QC is disabled and the test result signal 34 cannot be applied to the antenna 50 and no signal is radiated towards the test unit 12. Hence the coupler 68 and the test result signal 34 are synchronized to the antenna couple enable signal 170. The capacitor CC acts as a coupling capacitor to remove DC energy from the test result signal 34 and couple the test result signal 34 to the antenna 50.--

The paragraph beginning at page 28, line 23 has been amended as follows:

-- An alternative embodiment for transmitting the test result signal 34 to the test unit 12 involves modulating the impedance of the antenna 50 to re-radiate an RF signal that contains the information of the test result signal 34. Referring to Figure 27, a partial view of the test circuit 14 shows that the alternative embodiment implementation of the coupler 66 68 includes synchronization and coupling features. The coupler 68 includes two transistors QC1 and QC2 that are connected in series. The transistor QC2 acts as both a synchronization element and as a coupler to couple the transistor QC1, the impedance of which encodes the test result signal 34, to the antenna 50. The transistor QC2 is controlled by the antenna couple enable signal 170 in the same fashion described for an the embodiment shown in Figure 26. The test result signal 34 is used to control the transistor QC1 which is connected such that it behaves like a resistor when enabled. When the test result signal 34 has a digital logic value of '1', the transistor QC1 is enabled and increases the resistance of the antenna 50. Conversely,

when the test result signal 34 has a digital logic value of '0', the transistor QC1 is disabled and the impedance of the antenna 50 returns to its original value. Since the periodic transition from a digital logic value of '1' to a digital logic value of '0' and vice-versa indicates the frequency of the test result signal 34, the frequency of the impedance modulation of the antenna 50 encodes the frequency information contained within the test result signal 34.--

The paragraph beginning at page 29, line 7 has been amended as follows:

-- In either of the aforementioned embodiments, if the test result signal 34 were coupled to the antenna 50 ~~via the coupler 66~~ without the antenna couple enable signal 170, the test unit 12 would see a series of frequencies but would not be able to easily determine which test state the test circuit 14 is currently in. To allow for synchronization between the test unit 12 and the test circuit 14, the sequencer 60 also switches the ~~coupler 66~~ synchronization element 66 shown in Figure 26 or the transistor QC2 in the coupler 68 shown in Figure 27 so that before each repetition of the test sequence, i.e. during test state 0 or 8, the coupler ~~66~~ 68 is disabled so that no signal is radiated towards the test unit 12. The test unit 12 may therefore synchronize to the test result signal 34 by the absence of reception of the test result signal 34 from the test circuit 14.-

The paragraph beginning at page 29, line 28 has been amended as follows:

-- Referring to Figure 28, a modification of the test circuit 14 which would allow the test circuit 14 to test a sub-circuit 180 within the IC 18 is shown. This embodiment includes the circuitry shown in Figure 7 as well as an enable transistor QE connected to ground VSS, a test signal 182 and an enable test sub-circuit signal 184. The source voltage VDD which is used to power the sub-circuit 180 is provided by the voltage rectifier 52. The power of the sub-circuit 180 is provided by the enable test sub-circuit signal 184 that grounds the sub-circuit 180. This grounding is required because a ground path is needed before the sub-circuit 180 can be powered. This embodiment is preferable because there is a low voltage drop across the transistor QE. In this configuration, the sequencer 60 is modified to provide the enable test sub-circuit signal 184 as well as the test signal 182 that is used to test the functionality of the sub-circuit 180. The test signal 182 can be used to set one or many logic states within the sub-circuit 180. The resulting output signal of the sub-circuit 180, i.e. the test result signal 34, is then sent to the coupler 68. The coupler 68 also receives the antenna couple enable signal 170 which was previously described in the alternative embodiment shown in Figure 27 (alternatively, the embodiment having the synchronization element 66 and the coupler 68 shown in Figure 26 may also be used for synchronization and coupling). The test result signal 34 may then be transmitted to the test unit 12 where the test result signal 34 may be evaluated to determine whether the sub-circuit 180 behaved correctly.--